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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/802,857	KOH ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,28,40 and 45-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27,28,40 and 45-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to Applicant's submission filed on October 1, 2007. Claims 27, 28, 40 and 45-52 are now pending.

Response to Amendment

2. The rejection of claims 31 and 37-39 under 35 U.S.C. 112, second paragraph, is withdrawn in view of Applicant's amendment.

Response to Arguments

3. Applicant's arguments with respect to claims 27, 28 and 40 have been fully considered but they are not persuasive.

Applicant's assertion that "Sagane and Suzuki, either individually or as a whole, fail to disclose, teach, or suggest a bug address setting register adapted to store a bug address, said bug address indicating an address for buggy data" (remarks, page 9) is merely a conclusion without any supporting rationale. As set forth in the Office action, Sagane teaches an interrupt generating address register 9 in FIG. 1. The register stores a correction or bug address (see, for example, column 3, lines 40-43) that indicates a starting address for a buggy part of the program (see, for example, column 3, lines 32-39). Thus, Sagane teaches a bug address setting register adapted to store a bug address, said bug address indicating an address for buggy data.

Applicant contends, "Suzuki fails to disclose, teach, or suggest that [the] number of correcting portions is incremented by 1," and states, "Instead, Suzuki merely teaches that the stored number of correcting portions S is decremented" (remarks, page 10).

However, the examiner respectfully submits that the Office action establishes a *prima facie* case of obviousness. Suzuki teaches storing a value that represents the number of correcting portions S (step S5 in FIG. 4A). Suzuki further teaches that during the "processing to set [the] ROM correction data for [the] next correcting portion," the stored value is decremented (step S28 in FIG. 4B). Then, the stored value is checked to determine whether or not the number of correcting portions is equal to 0 (step S29 in FIG. 4B). Suzuki states, "If the number of correcting portions S is 0, the processing goes to step S33 since there is no residual correcting portion in the subroutine module of code No. m ... [and] if the number of correcting portions S is not 0, the processing goes to step S30 since there [are] still residual correcting portions" (column 6, line 65 to column 7, line 2). Thus, Suzuki stores the value, decrements the stored value and checks whether or not the stored value is equal to 0 for the purpose of determining whether or not there are any correcting portions left to process. Indeed, Applicant's specification describes that "the counter register is increased by 1" for an analogous purpose, so that "the CPU 10 is able to judge the number of times of interrupt, that is, which number bug is being corrected, by the value of the counter register" (specification, page 26, lines 6-10). A person having ordinary skill in the art could implement the teachings of Suzuki such that the stored value is incremented rather than decremented and achieve the same results.

Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such as described in the Office action and achieve the intended results. Specifically, given the number of correcting portions S, a person having ordinary skill in the art could implement the teachings of Suzuki so as to initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored

value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in the reference, and its results are predictable. Thus, the claimed invention would have been obvious to a person having ordinary skill in the art.

In response to Applicant's argument that "the Office Action fails to show where within Suzuki there is taught that a specific amount by which the stored number of correcting portions S is decremented, or that the stored number of correcting portions S is decremented by 1" (remarks, page 11), Suzuki does teach that the stored value is decremented, as Applicant acknowledges, and it is implicit within these teachings that the stored value is decremented by 1. Applicant does not provide any evidence to the contrary. Moreover, the test for obviousness is not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The combined teachings of Sagane and Suzuki would have suggested the claimed invention to those of ordinary skill in the art.

The examiner does not agree with Applicant's contention that "the assertions and urgings presented within the Office Action amount to nothing more than an 'obvious-to-try' situation" (remarks, page 11). Nonetheless, Applicant is respectfully reminded that a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. See *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. ___, 82 USPQ2d 1385 (2007).

4. Applicant's arguments with respect to new claims 45-52 have been considered but are moot in view of the new ground(s) of rejection, as set forth below.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 45-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention.

With respect to claim 45, the claim recites the limitation "wherein said counter register is set to 0 during said initialization processing." There is insufficient antecedent basis for "said initialization processing" in the claim. Here, the examiner interprets the limitation as if the word "said" were omitted.

With respect to claims 46-52, the claims are dependent upon claim 45 and are therefore indefinite for at least the same reason(s) noted above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 27, 28 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,454,100 to Sagane (art of record, "Sagane") in view of U.S. Patent No. 5,784,537 to Suzuki et al. (art of record, "Suzuki").

With respect to claim 27 (currently amended), Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates an address for a buggy part of a program).

a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with the correction address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address (see, for example, column 5, lines 11-16, which shows that the interrupt request signal indicates coincidence or non-coincidence of the addresses);

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal (see, for example, CPU 2 in FIG. 1 and column 5, lines 16-21, which shows that the CPU processes an interrupt function upon receipt of the interrupt request signal).

Sagane does not expressly disclose:

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane, a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

With respect to claim 28 (previously presented), the rejection of claim 27 is incorporated, and Sagane in view of Suzuki further teaches or suggests that said value is incremented when said interrupt request signal indicates said coincidence (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value is incremented when said interrupt request signal indicates said coincidence.

With respect to claim 40 (currently amended), Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes (see, for example, ROM 3 in FIG. 1 and column 1, lines 9-14, which shows that the ROM is program memory that stores instruction codes as a program, and column 3, lines 48-52, which shows that an execution or program address indicates a location in the ROM);

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates a starting address within the ROM of a buggy part of the program).

Sagane further teaches an interrupt request signal that indicates a coincidence between said program address and said bug address (see, for example, column 3, lines 59-61, which shows an interrupt request signal, and column 3, lines 48-52, which shows that the interrupt request signal indicates a coincidence between the execution address and the correction address), but does not expressly disclose:

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane, a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

Sagane in view of Suzuki further teaches or suggests:

wherein another program address indicates a location within said program memory for another of the instruction codes (see, for example, column 3, lines 48-52, which shows that another execution or program address indicates another location in the ROM), and

wherein said value of the counter register is incremented by 1 (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value of the counter register is incremented by 1.

9. Claims 45-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sagane in view of U.S. Patent No. 6,412,081 to Koscal et al. (art of record, "Koscal") and in view of Suzuki.

With respect to claim 45 (new), Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes (see, for example, ROM 3 in FIG. 1 and column 1, lines 9-14, which shows that the ROM is program memory that stores instruction codes as a program, and column 3, lines 48-52, which shows that an execution or program address indicates a location in the ROM);

a central processing unit adapted to process interrupt functions, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal (see, for example, CPU 2 in FIG. 1 and column 5, lines 16-21, which shows that the CPU processes an interrupt function upon receipt of an interrupt request signal).

Sagane does not expressly disclose that the central processing unit is adapted to process interrupt functions of different priority levels.

Nonetheless, central processing units are known to process interrupt functions of different priority levels. For example, in an analogous art, Koscal teaches processing interrupt functions to patch bugs in a program (see, for example, the abstract). Koscal further teaches that the microprocessor executes interrupt functions of different priority levels (see, for example, column 14, lines 2-7).

Therefore, as Koscal suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane such that the central processing unit is adapted to process interrupt functions of different priority levels.

Sagane in view of Koscal further teaches or suggests:

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with a correction or bug address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said central processing unit receiving said first interrupt request signal (see, for example, FIG. 1, which shows that the CPU receives the interrupt request signal via interrupt control circuit 7d);

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with a correction or bug address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said central processing unit receiving said second interrupt request signal (see, for example, FIG. 1, which shows that the CPU receives the interrupt request signal via interrupt control circuit 7d).

Sagane teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). In an analogous embodiment, Sagane similarly teaches a correction address register that is updated to reflect the next correction address (see, for example, column 6, lines 63-67), and further suggests, as an alternative, providing a plurality of correction address registers and a plurality of comparators for the plurality of buggy parts (see, for example, column 6, line 67 to column 7, line 3). A person having ordinary skill in the art at the time the

invention was made could incorporate a plurality of comparators into the data processing apparatus of Sagane with predictable results.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Koscal such that it comprises first and second coincidence detecting circuits adapted to compare said program address with first and second bug addresses and output said first and second interrupt request signals, respectively.

Sagane further teaches that the interrupt request signal indicates a coincidence between said program address and said first bug address or a coincidence between said program address and said second bug address (see, for example, column 3, lines 48-52, which shows that the interrupt request signal indicates a coincidence between the execution address and the correction address), but Sagane and Koscal do not expressly disclose:

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). As noted above, Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction

address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane and Koscal, a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said first bug address or a coincidence between said program address and said second bug address.

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the

value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal and Suzuki such that said value is incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address, wherein said counter register is set to 0 during said initialization processing.

With respect to claim 46 (new), the rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said counter register is located within a random access memory at a predetermined memory address (see, for example, Suzuki, column 5, lines 41-46, which shows that the value is stored at a predetermined location in RAM).

With respect to claim 47 (new), the rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests:

bug address setting registers adapted to store said first and second bug addresses (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores the correction or bug address).

With respect to claim 48 (new), the rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said first bug address indicates a

starting address within said program memory for a first buggy part of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program (see, for example, column 3, lines 32-39, which shows that that the correction or bug addresses indicate starting addresses within the ROM of buggy parts of the program).

With respect to claim 49 (new), the rejection of claim 48 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part (see, for example, Suzuki, column 6, line 65 to column 7, line 7, which shows that the value is used to select the corresponding buggy part for correction).

With respect to claim 50 (new), the rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches that said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals (see, for example, column 5, lines 49-54, which shows that the interrupt request signal is generated separately for each buggy part of the program).

10. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sagane in view of Koscal and in view of Suzuki, as applied to claim 45 above, and further in view of U.S. Patent No. 5,701,506 to Hosotani (art of record, "Hosotani").

With respect to claim 51 (new), the rejection of claim 45 is incorporated. Sagane, Koscal and Suzuki do not expressly disclose that said first and second interrupt request signals are input to said central processing unit as a single interruption.

However, in an analogous art, Hosotani teaches a plurality of coincidence detecting circuits that each output a signal indicating a coincidence between a program address and a bug address (see, for example, match circuits 9 in FIG. 2 and column 4, lines 30-59). Hosotani further teaches that the coincidence signals are combined into a single signal (see, for example, column 4, line 60 to column 5, line 2). The teachings of Hosotani enable, for example, correcting a plurality of bugs in a program stored in a ROM without remaking the ROM (see, for example, column 1, lines 45-50).

Therefore, as Hosotani suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal and Suzuki such that said first and second interrupt request signals are input to said central processing unit as a single interruption, so as to provide an optimized approach to correcting a plurality of bugs in a program.

With respect to claim 52 (new), the rejection of claim 51 is incorporated, and Sagane in view of Koscal, Suzuki and Hosotani further teaches or suggests that said first and second interrupt request signals are AND'ed together to become said single interruption.

Hosotani teaches that the coincidence signals are OR'ed together, and that the resulting output is at a "1" level when any one of the address comparisons is a match and at a "0" level when all of the comparisons are mismatches (see, for example, column 4, line 60 to column 5,

line 2). In other words, Hosotani defines the coincidence detection mechanism as "active high." When the mechanism is instead defined as "active low," a person having ordinary skill in art could substitute the OR gate 14 with an AND gate to achieve the same result. The resulting output from the AND gate, in this case, would be at a "0" level when any one of the address comparisons is a match and at a "1" level when all of the comparisons are mismatches.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal, Suzuki and Hosotani such that said first and second interrupt request signals are AND'ed together to become said single interruption.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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